ABSTRACT

Disclosed is a sense amplifier arrangement that achieves high-speed access and shorter cycle time when array voltage is lowered in a DRAM. In a TG clocking sense system to separate data lines between the array side and the sense amplifier side in an early stage of a sensing period, a restore amplifier RAP is added, which amplifies data lines on the array side by referring to the data in the sense amplifier, and the restore amplifier is driven by a voltage VDH higher than the array voltage VDL. As a result, high-speed sense operation of the TG clocking system is made compatible with high-speed restore operation of overdrive system, and it is possible to achieve high-speed access operation and shorter cycle time.